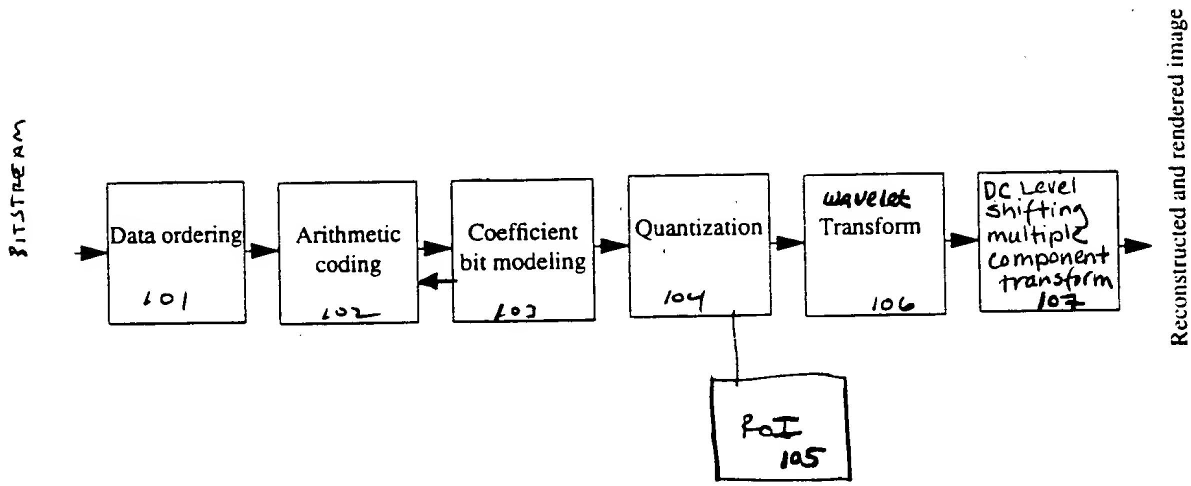

BITSTREAM
Data ordering
101
Arithmetic coding
102
Coefficient bit modeling
103
Quantization
104
RoI
105
wavelet Transform
106
DC Level shifting multiple component transform
107
Reconstructed and rendered image

Figure 1

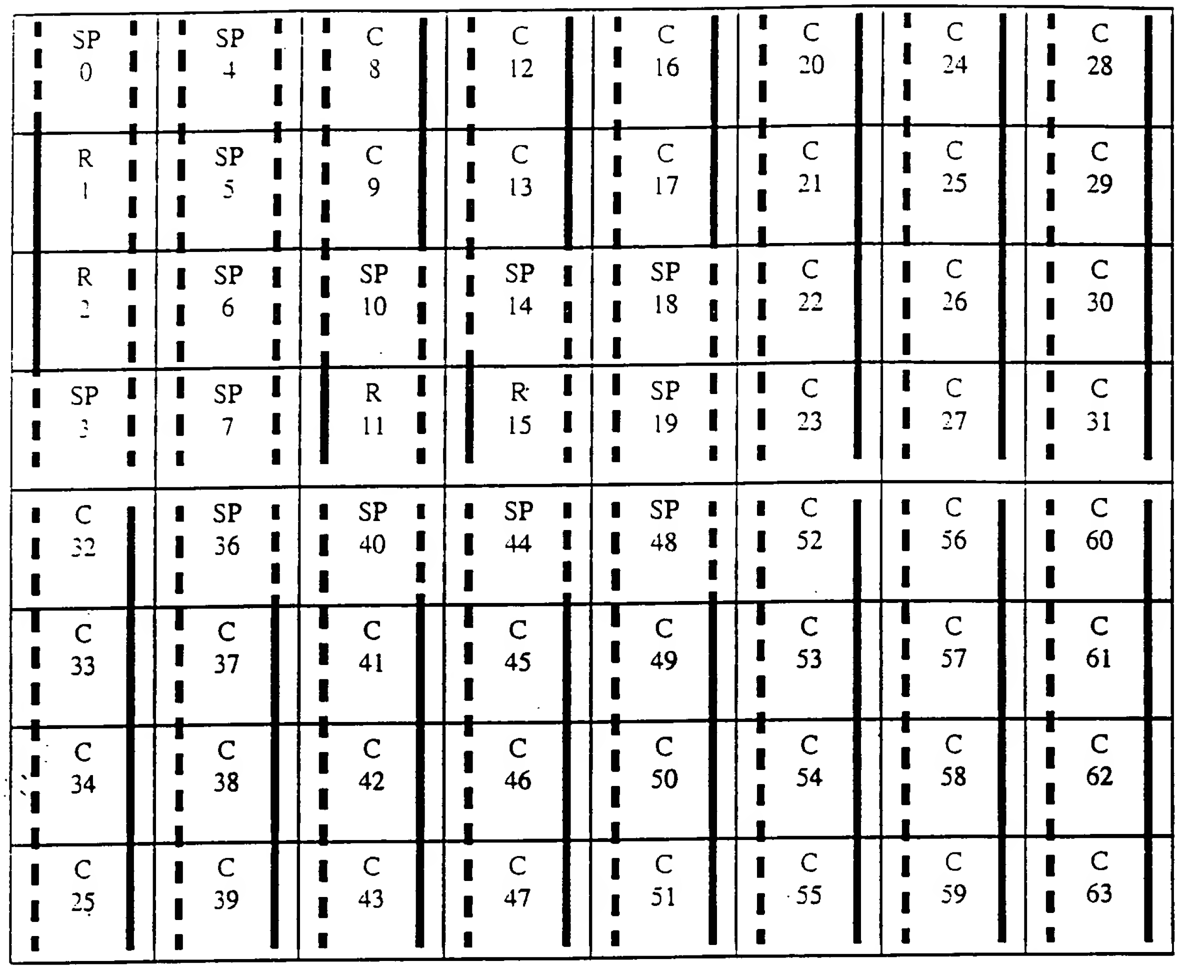

SP 0
SP 4
C 8
C 12
C 16
C 20
C 24
C 28
R 1
SP 5
C 9
C 13
C 17
C 21
C 25
C 29
R 2
SP 6
SP 10
SP 14
SP 18
C 22
C 26
C 30
SP 3
SP 7
R 11
R 15
SP 19
C 23
C 27
C 31
C 32
SP 36
SP 40
SP 44
SP 48
C 52
C 56
C 60
C 33
C 37
C 41
C 45
C 49
C 53
C 57
C 61
C 34
C 38
C 42
C 46
C 50
C 54
C 58
C 62
C 25
C 39
C 43
C 47
C 51
C 55
C 59
C 63

Figure 2A

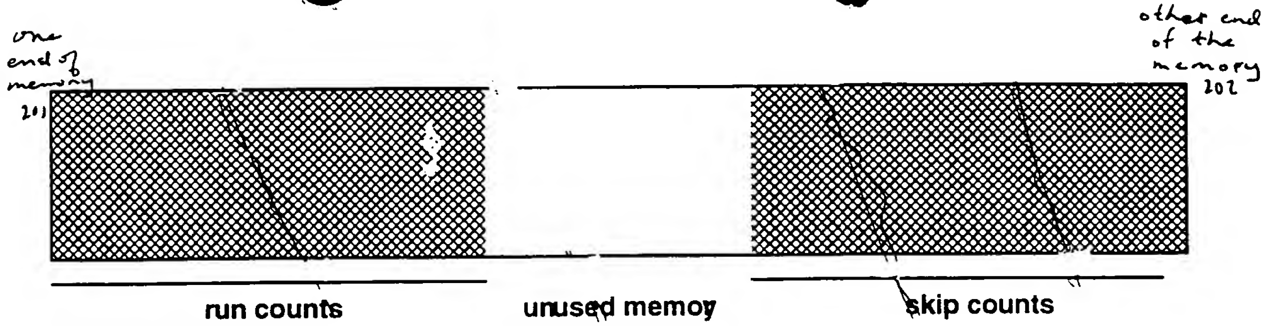


Figure 2B

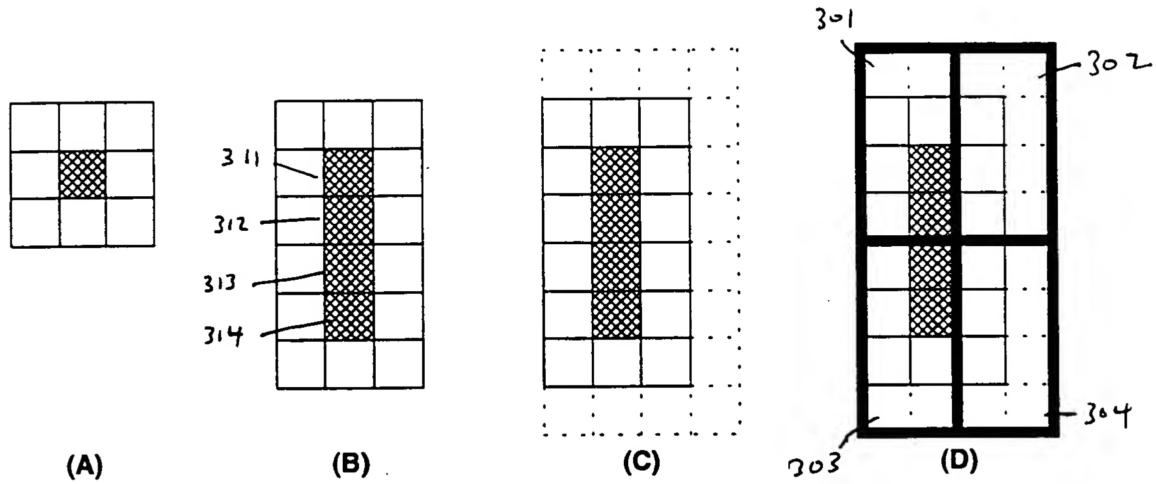


Figure 3

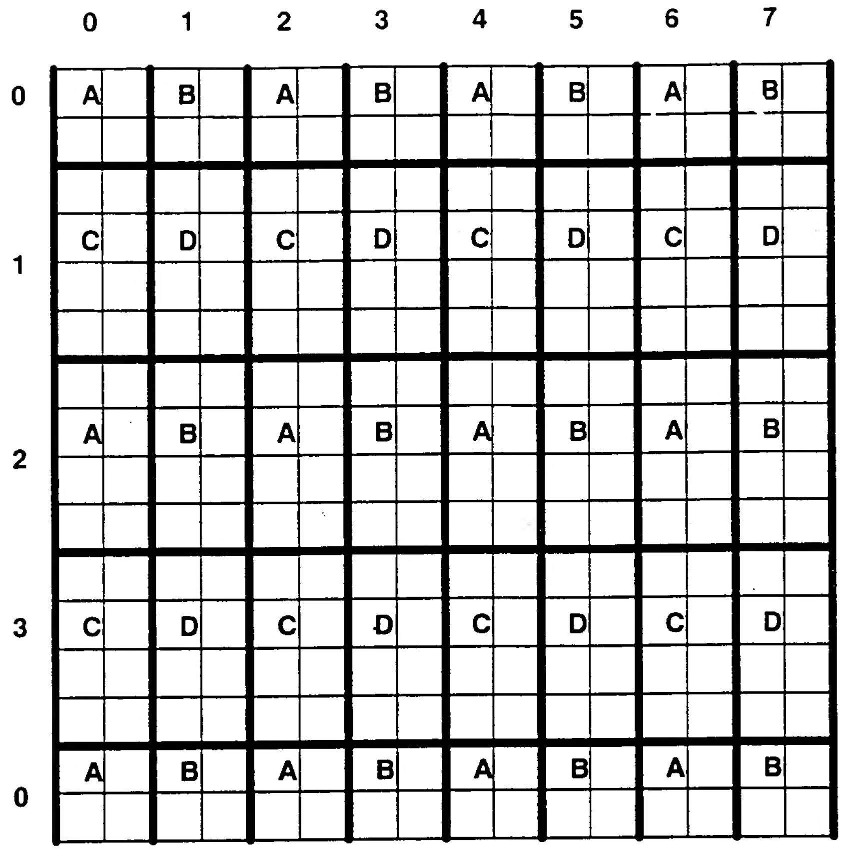

0 1 2 3 4 5 6 7
0 A B A B A B A B
1 C D C D C D C D
2 A B A B A B A B
3 C D C D C D C D
0 A B A B A B A B

Figure 4

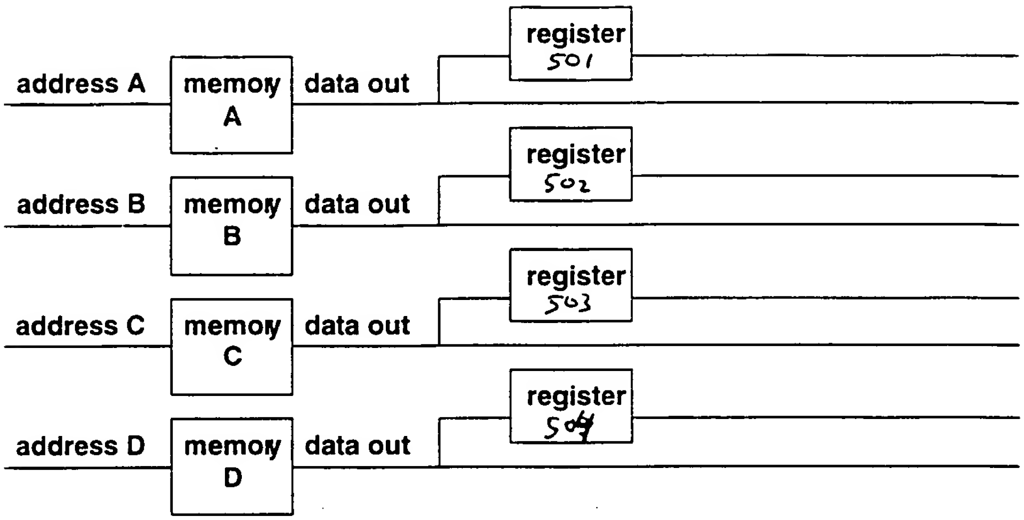


Figure 5

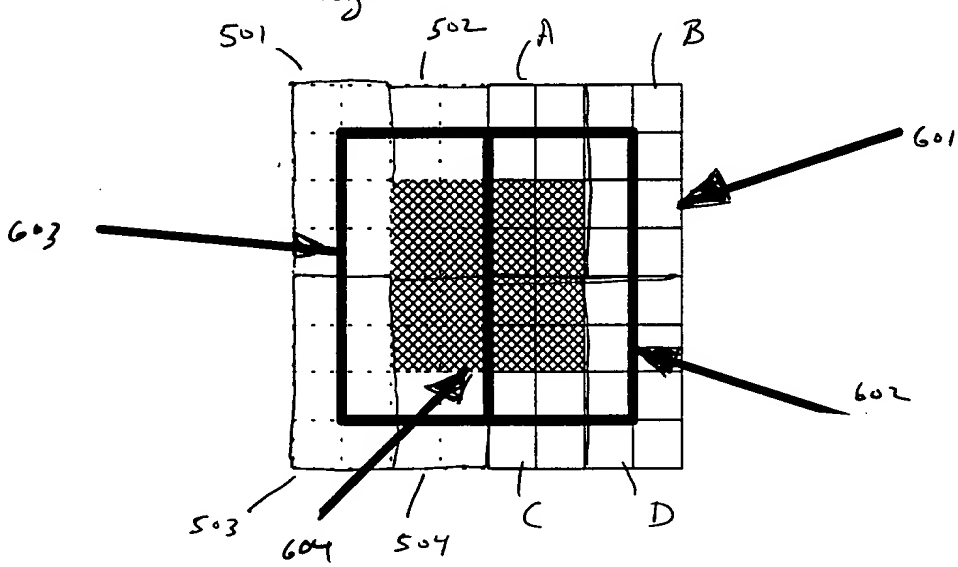


Figure 6

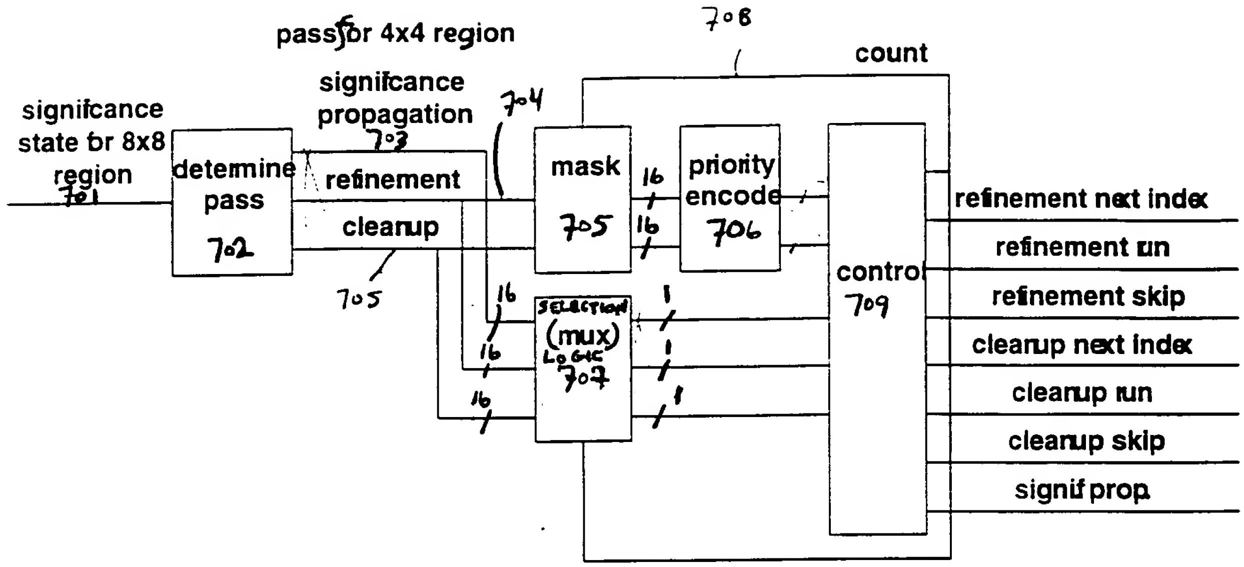


Figure 7

SP	SP	SP	SP
C	C	C	C
SP	SP	SP	SP
SP	R	R	SP

SP = significance propagtion
C = cleanup
R = refinement

SP pass: 10*2 for SP pass coefficients
6 for C and R pass coefficients
C pass: 4*2 for C pass coeficients
R pass: 2 for R pass

total: 36 clocks = 2.25 clocks per coefficient

Figure 8

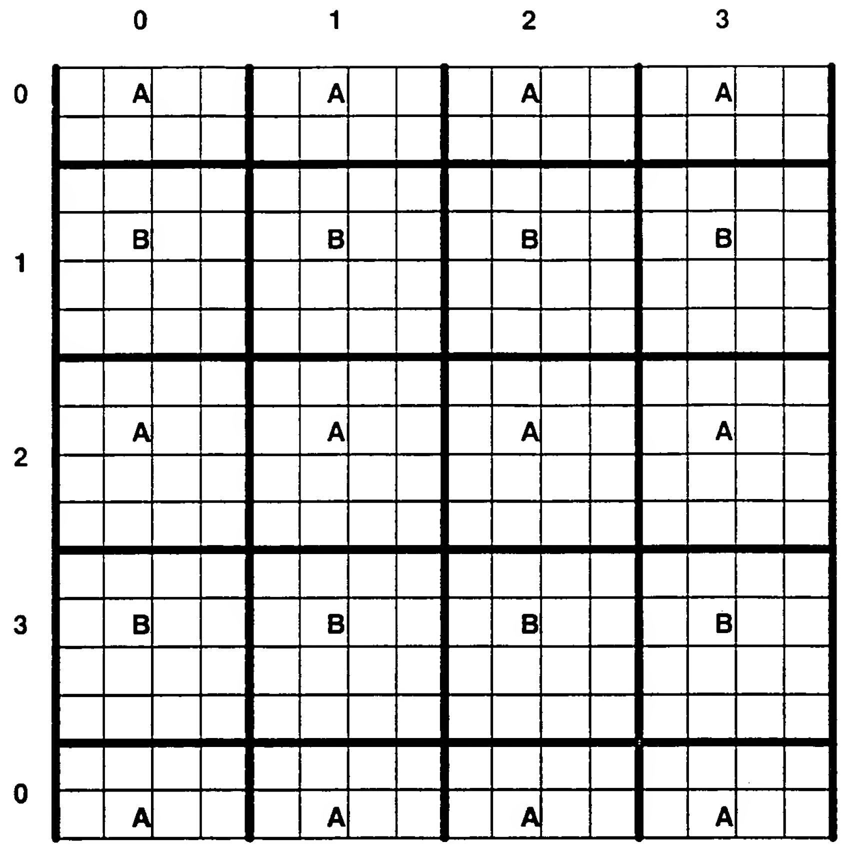


Figure 9

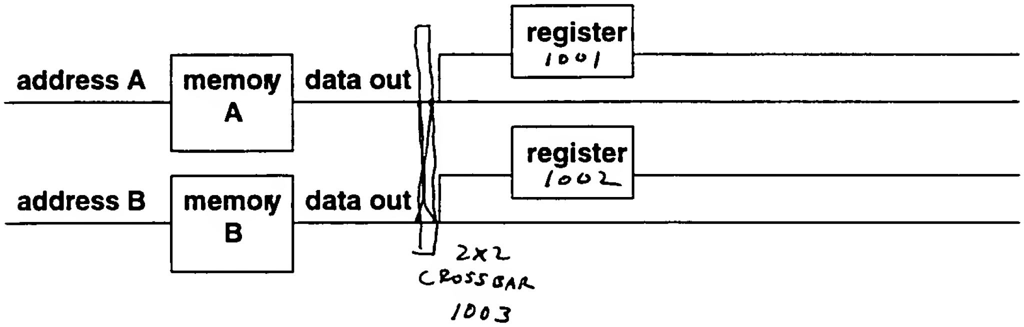


Figure 10

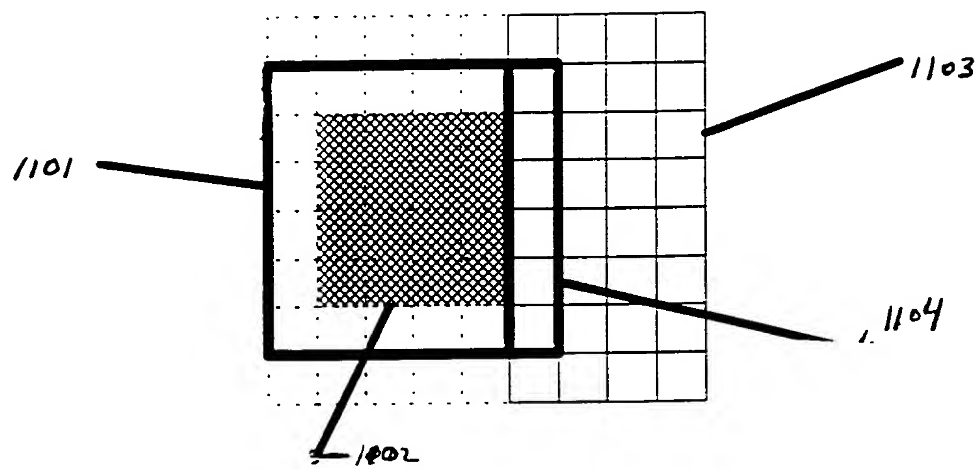


Figure 11

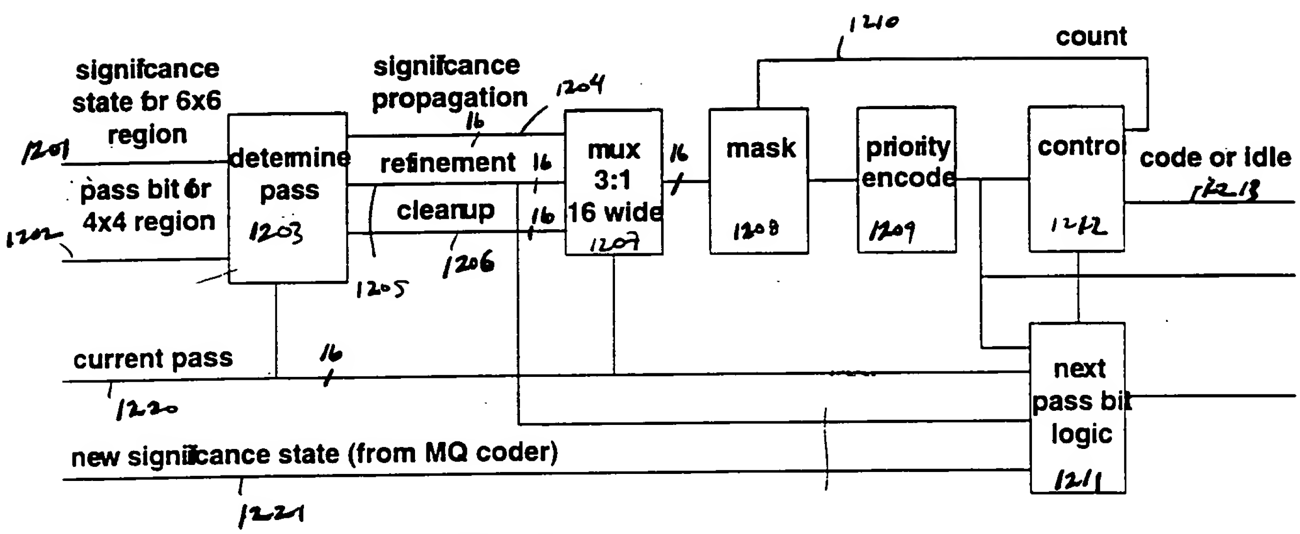


Figure 12

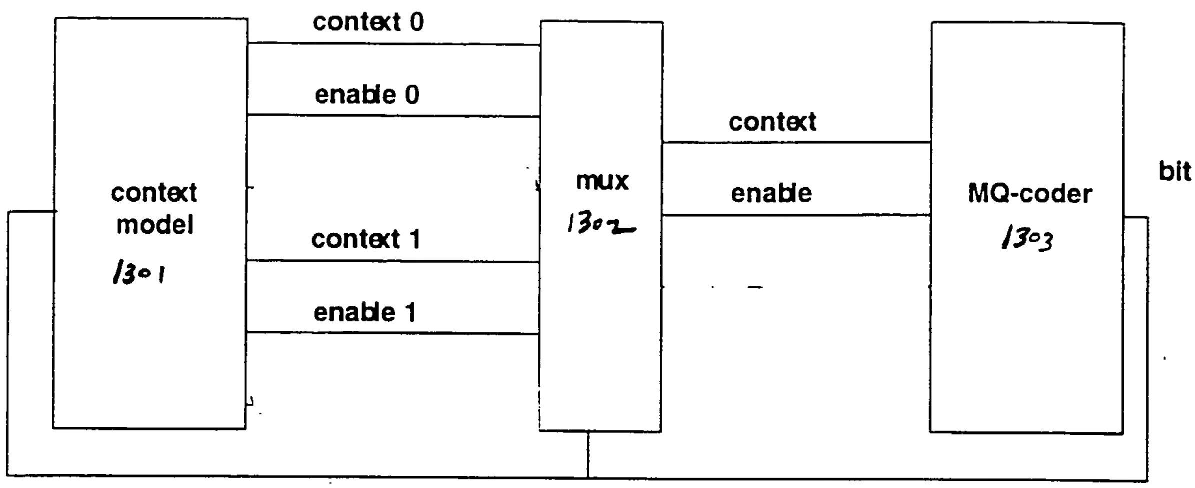


Figure 13

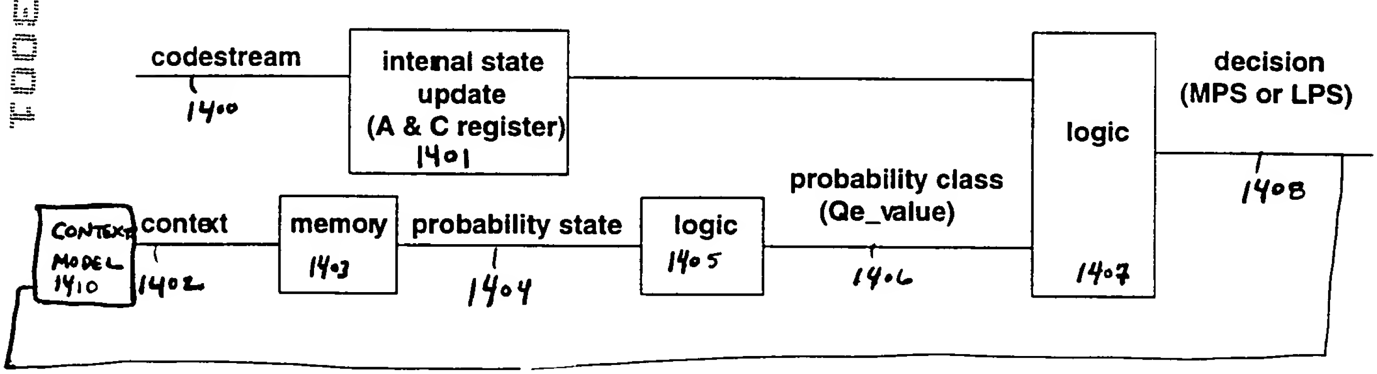


Figure 14A

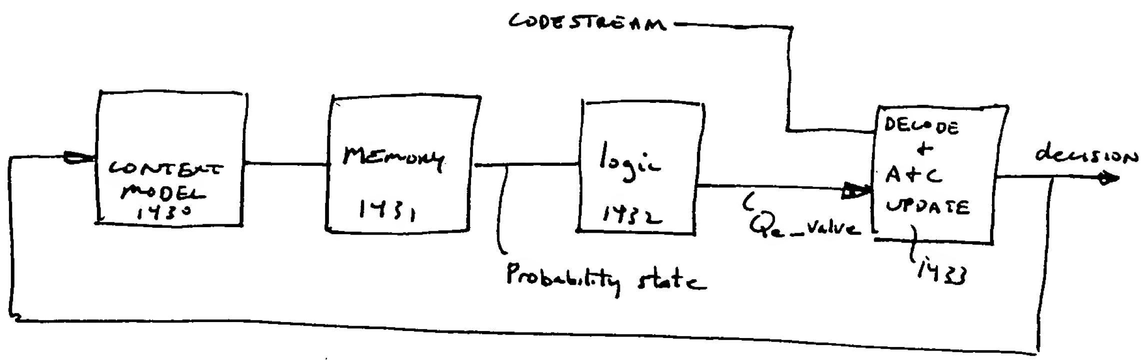

CODESTREAM
CONTEXT MODEL 1430
MEMORY 1431
logic 1432
DECODE + A+C UPDATE
1433
decision
Qe_value
Probability state

Figure 14B.

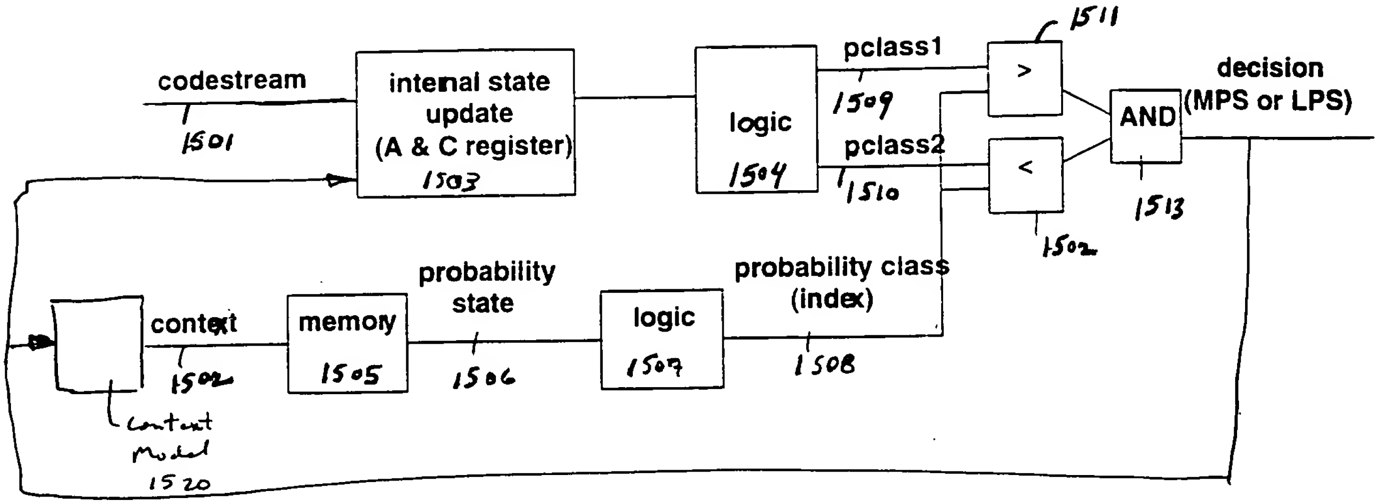


Figure 15

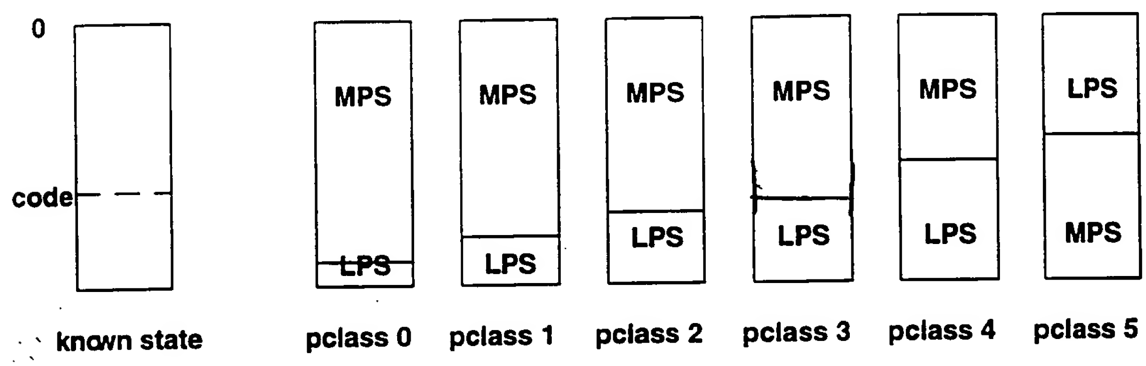


Figure 16A

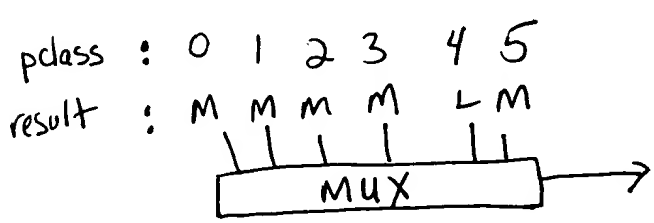


Figure 16B

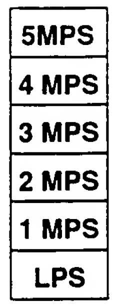


Figure 17

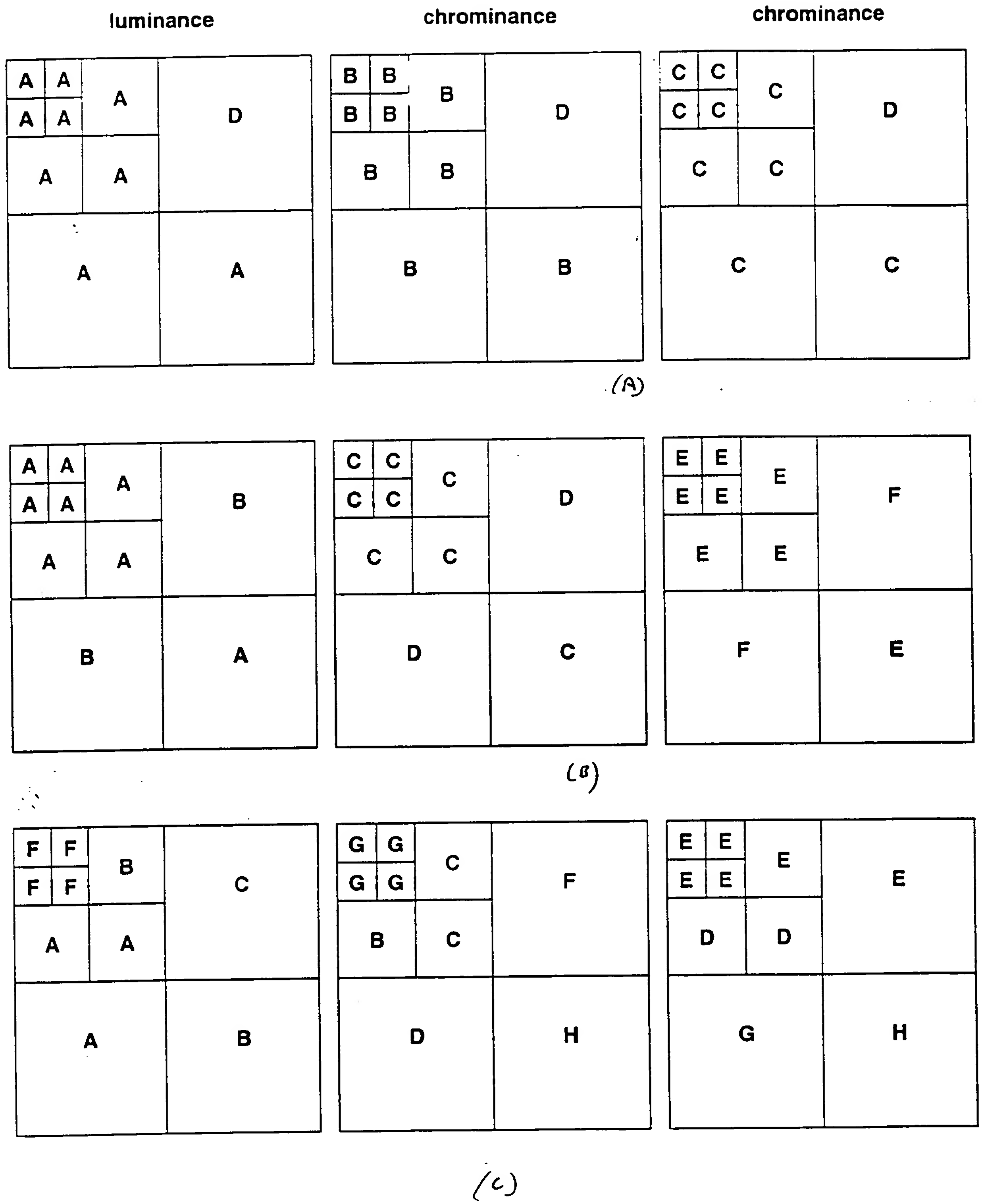


Figure 18

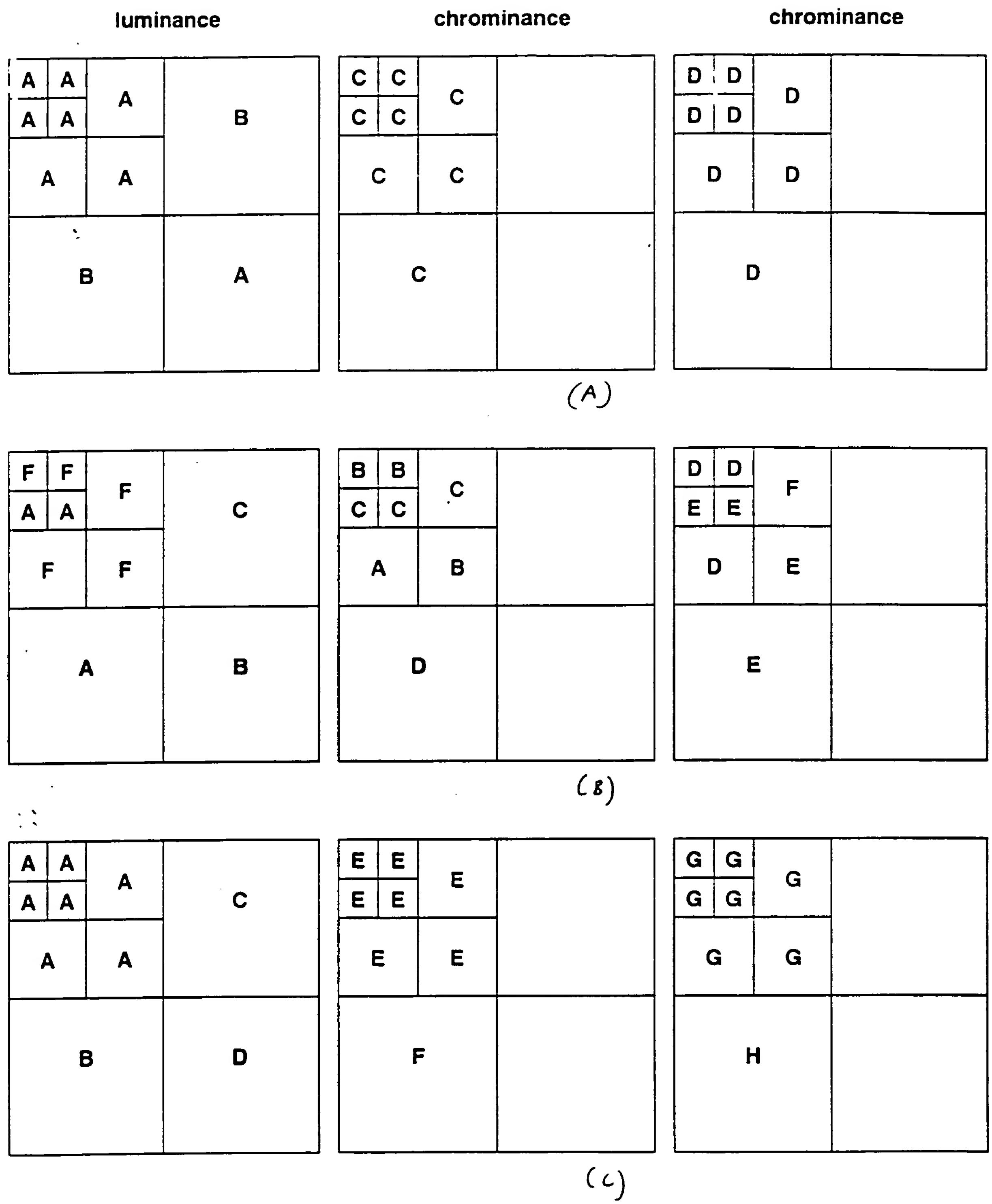


Figure 19

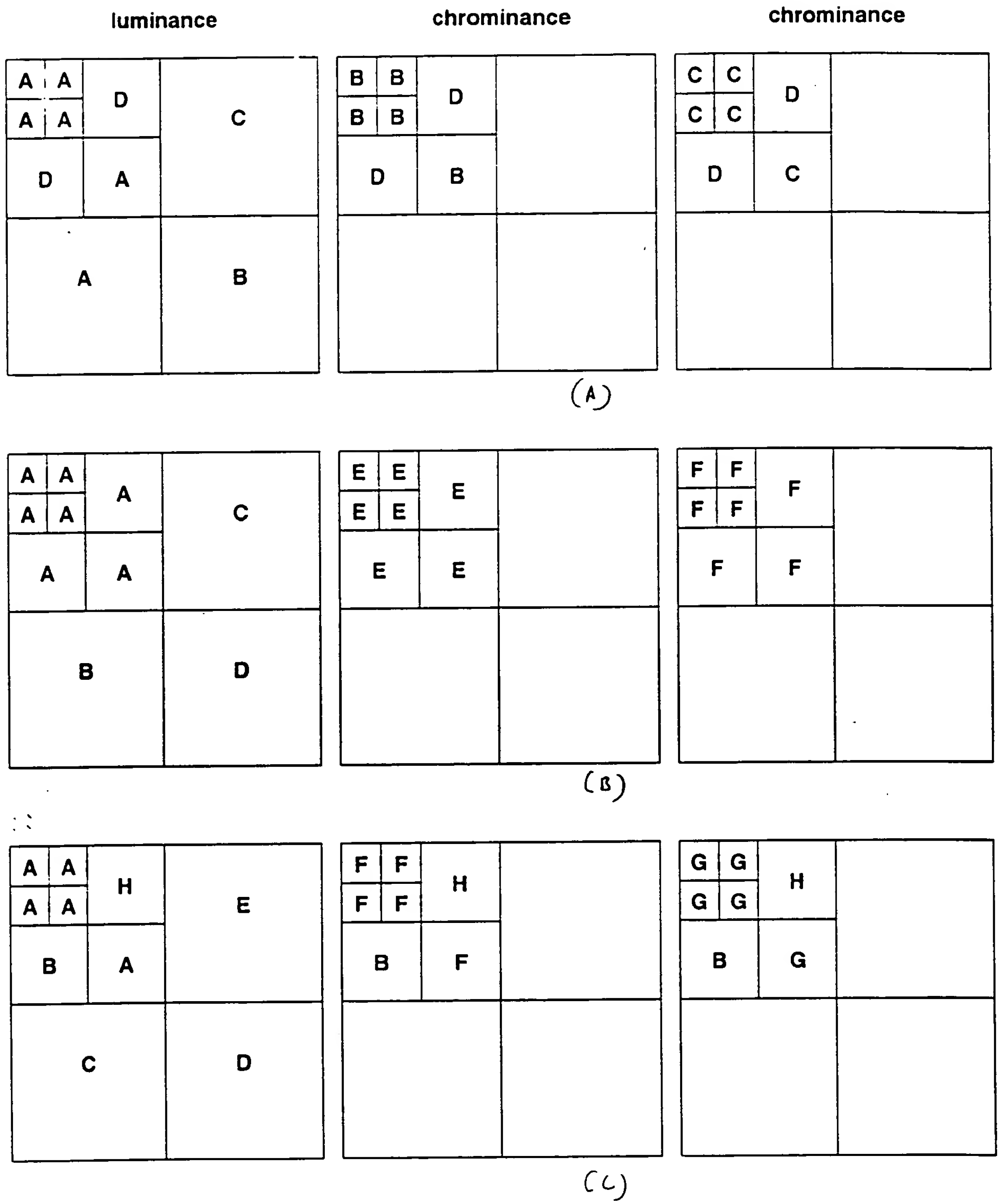

luminance
chrominance
chrominance
A A A A D C D A A B
B B B B D D B
C C C C D D C
(A)
A A A A A C A A B D
E E E E E E E
F F F F F F F
(B)
A A A A H E B A C D
F F F F H B F
G G G G H B G
(C)

Figure 20

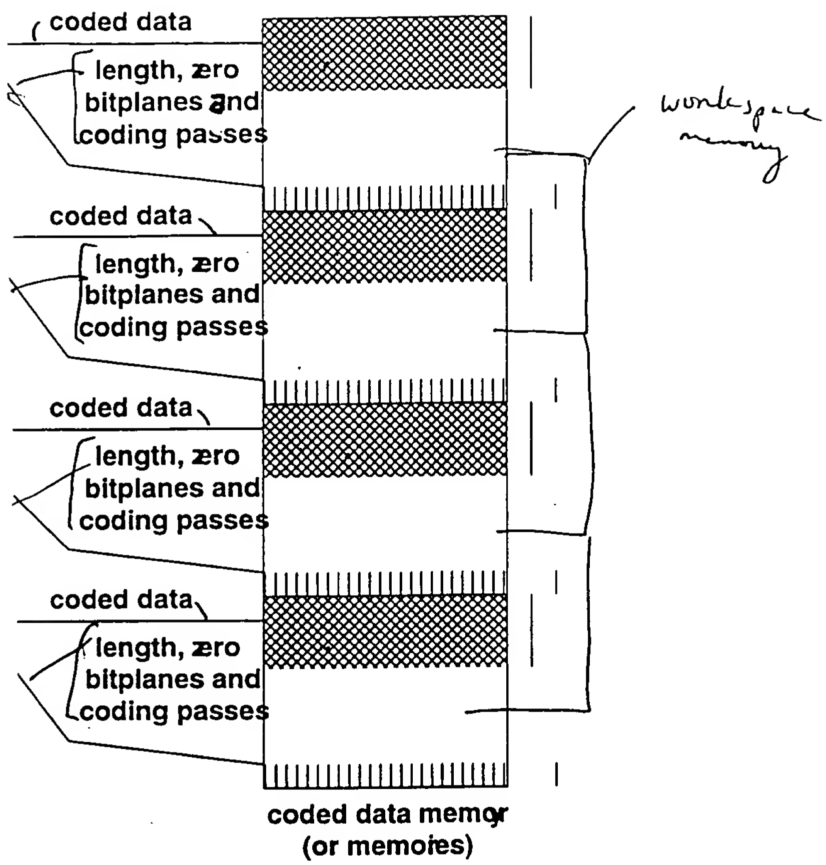

coded data
length, zero bitplanes and coding passes
coded data
length, zero bitplanes and coding passes
coded data
length, zero bitplanes and coding passes
coded data
length, zero bitplanes and coding passes
workspace memory
coded data memory (or memories)

Figure 21

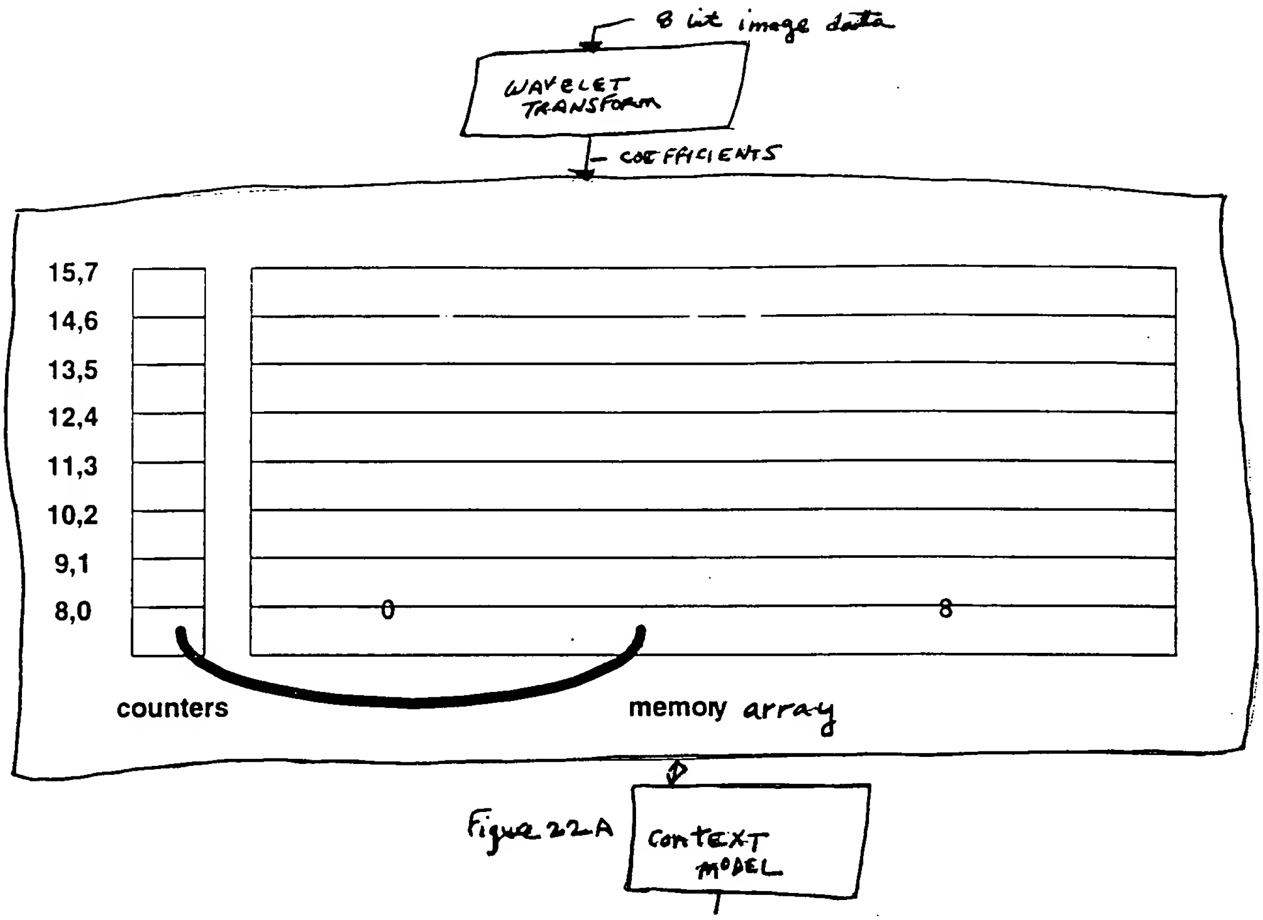


Figure 22A

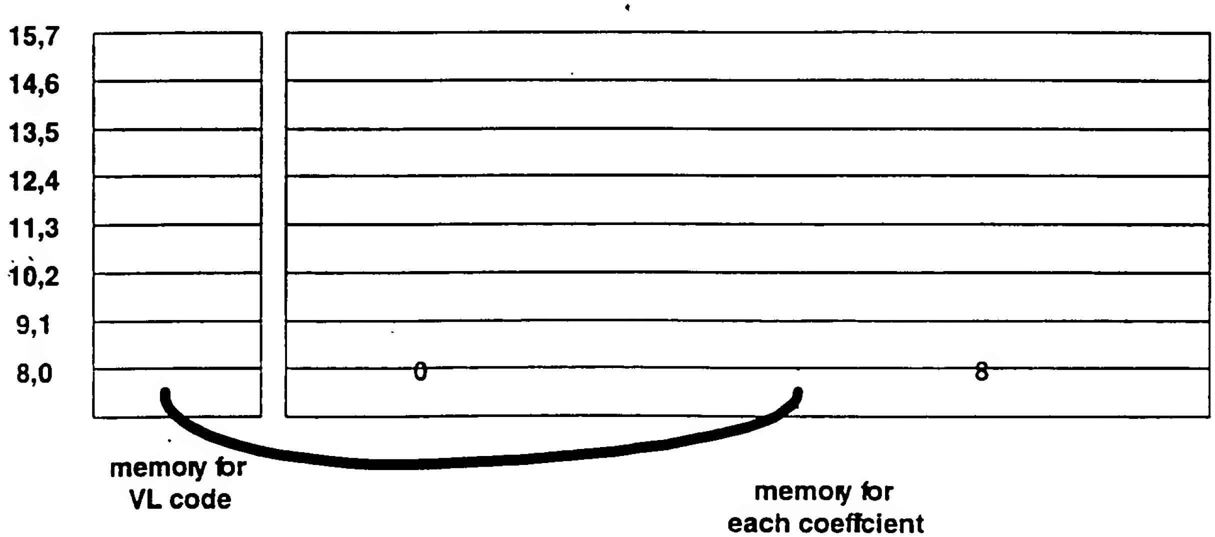
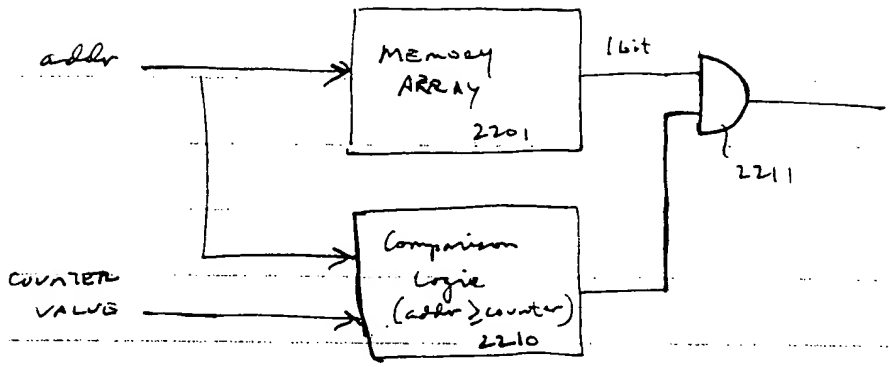
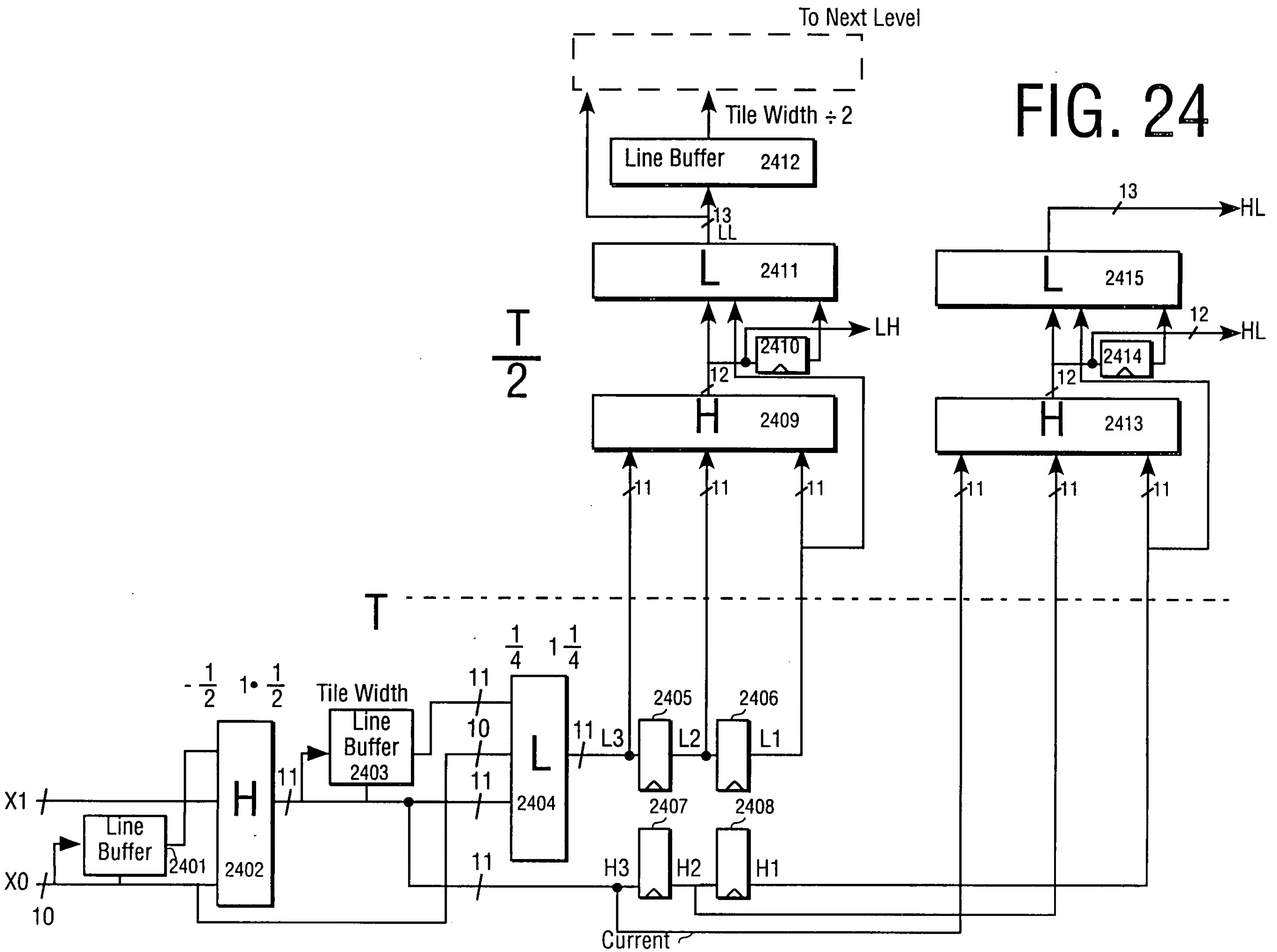


Figure 23



addr
MEMORY ARRAY
2201
1 bit
2211
COUNTER VALUE
Comparison Logic (addr ≥ counter)
2210

Figure 22B



To Next Level
Tile Width ÷ 2
Line Buffer 2412
13
LL
L 2411
LH
2410
12
H 2409
11
11
11
L 2415
13
HL
12
HL
2414
12
H 2413
11
11
11
T/2
T
X1
X0
10
Line Buffer
2401
-1/2
1• 1/2
H
2402
11
Tile Width
Line Buffer 2403
11
10
11
11
1/4
1 1/4
L
2404
11
L3
L2
L1
2405
2406
2407
2408
H3
H2
H1
Current

FIG. 24

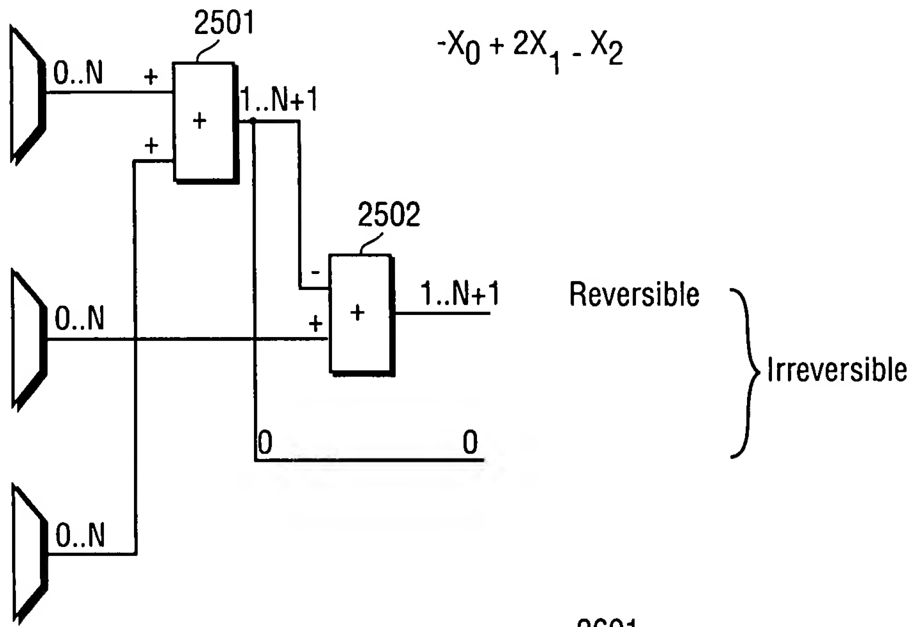


FIG. 25A

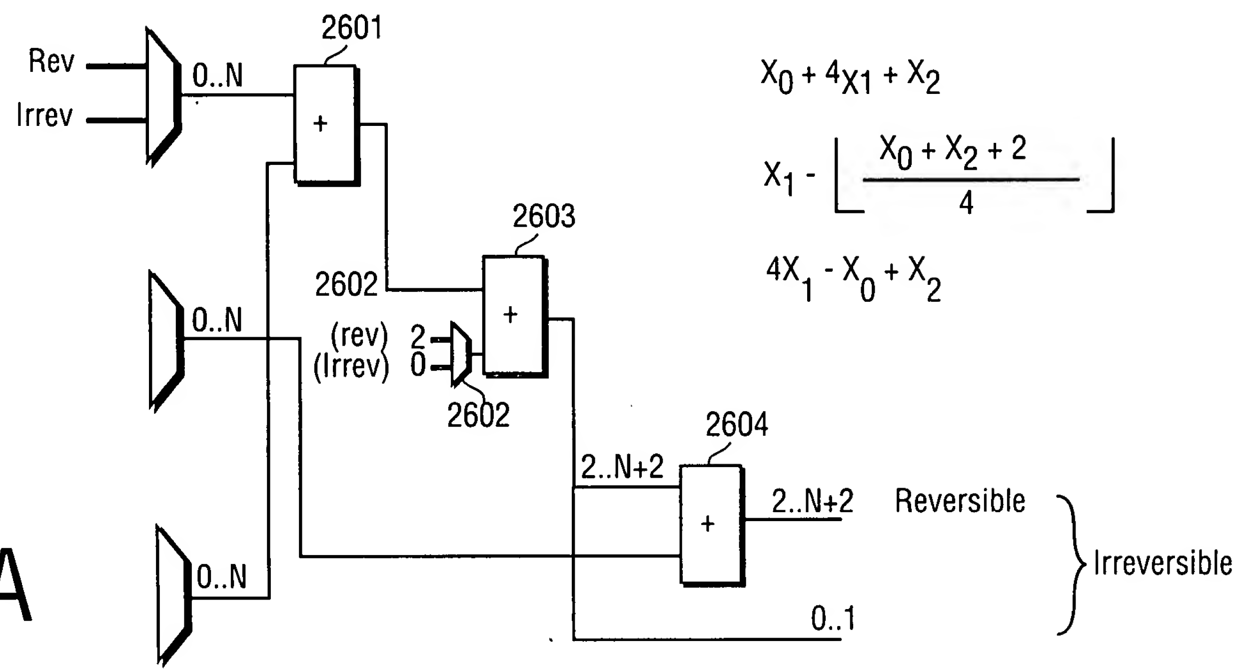


FIG. 26A

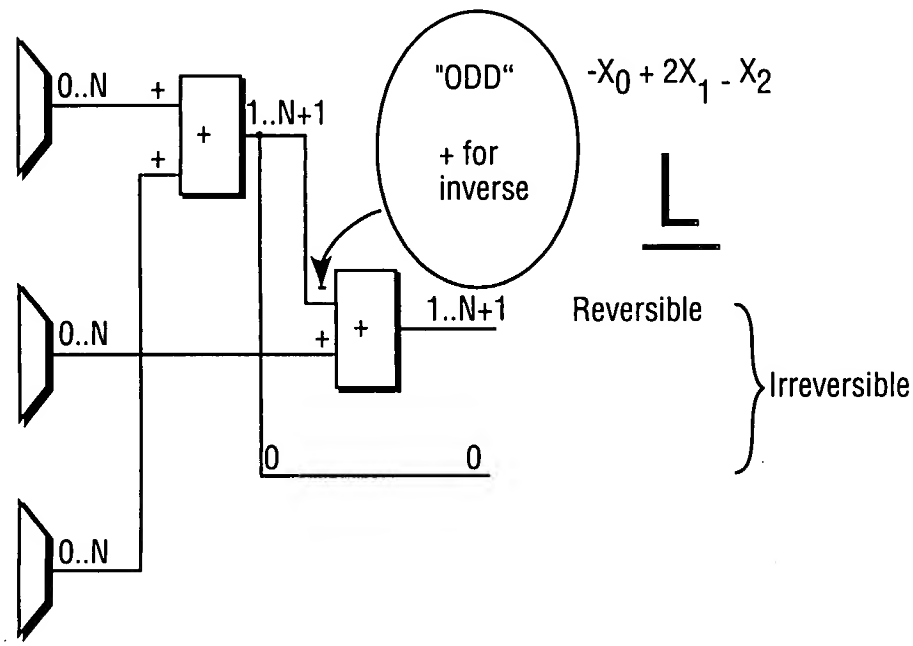


FIG. 25B

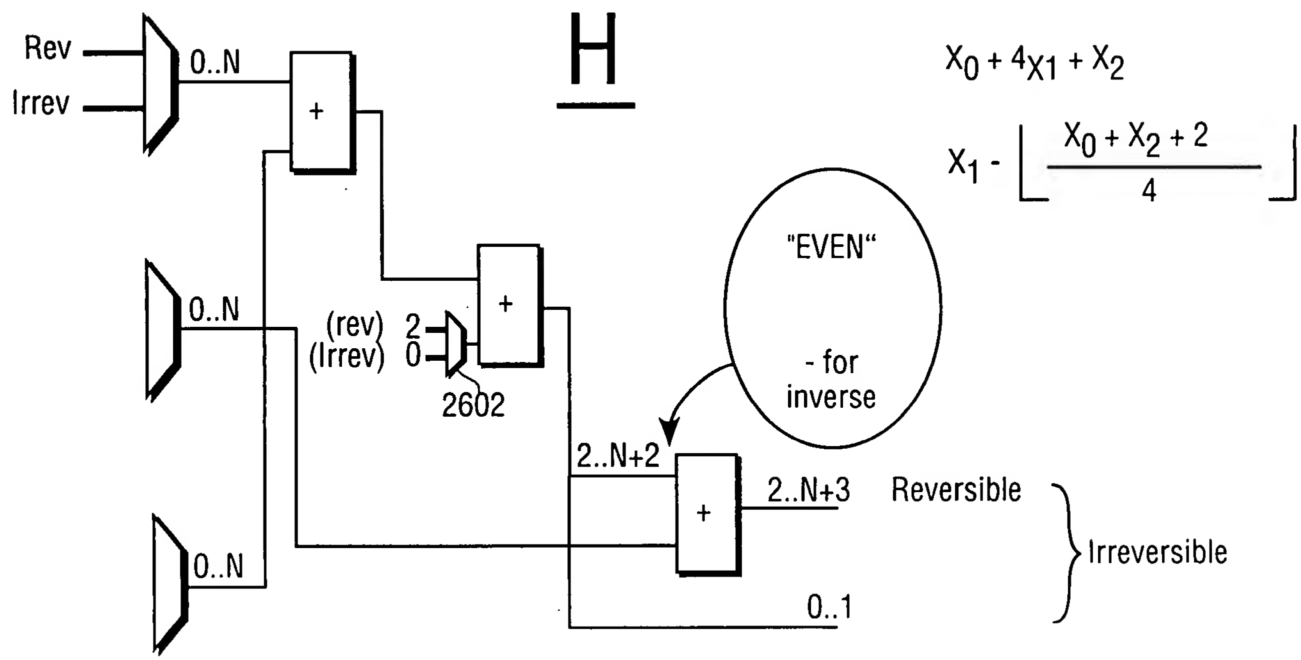
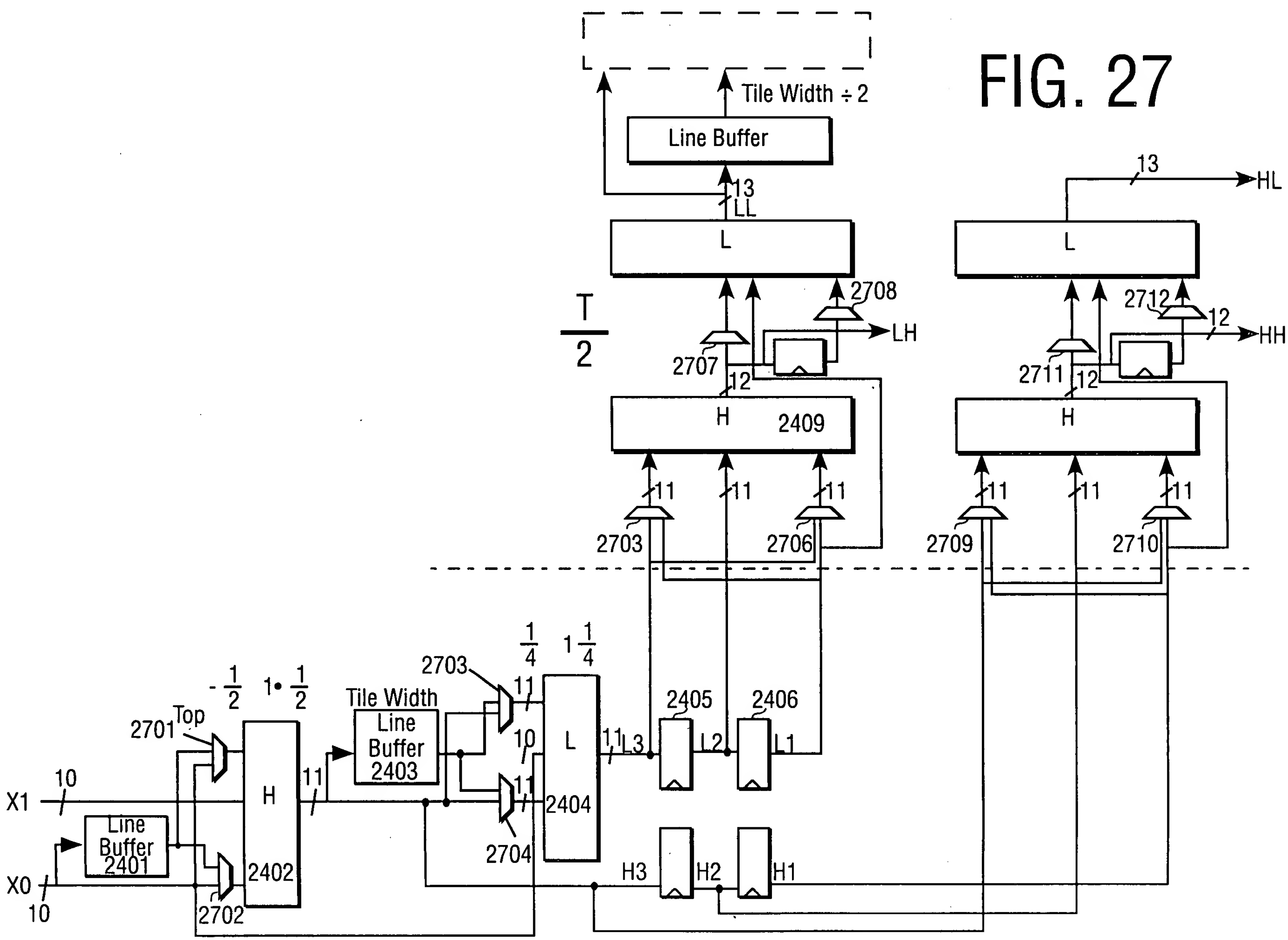


FIG. 26B



Tile Width ÷ 2
Line Buffer
13
LL
L
T/2
2708
LH
2707
12
H
2409
11
2703
2706
13
HL
2712
12
HH
2711
2709
2710
-1/2
1• 1/2
1/4
1 1/4
2701
Top
2702
2402
Tile Width
Line Buffer
2403
2704
2404
10
X1
X0
Line Buffer
2401
2405
2406
L3
L2
L1
H3
H2
H1

FIG. 27

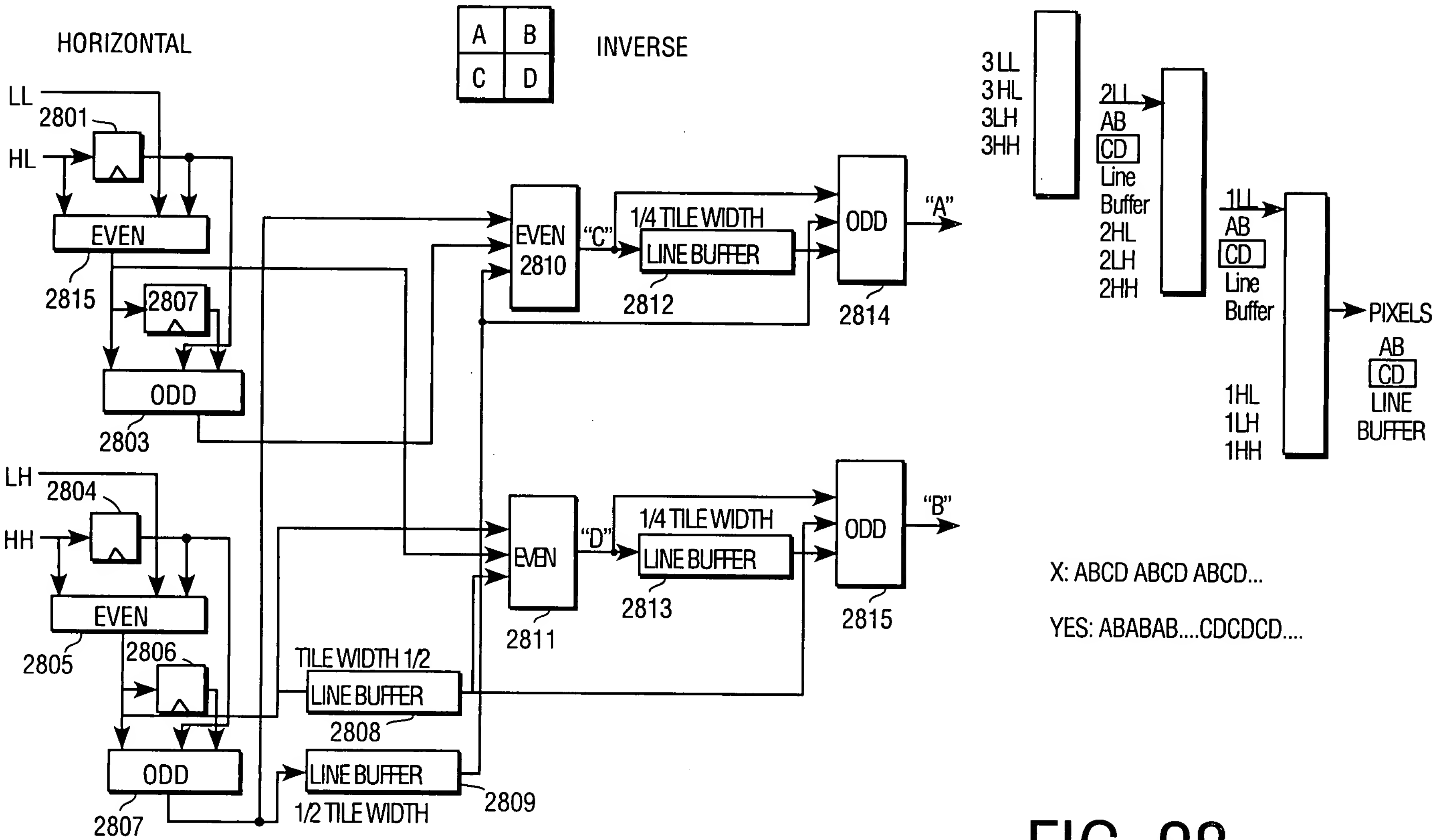

HORIZONTAL
A
B
C
D
INVERSE
LL
HL
2801
EVEN
2815
2807
ODD
2803
LH
HH
2804
EVEN
2805
2806
ODD
2807
TILE WIDTH 1/2
LINE BUFFER
2808
LINE BUFFER
1/2 TILE WIDTH
2809
EVEN
2810
"C"
1/4 TILE WIDTH
LINE BUFFER
2812
ODD
2814
"A"
EVEN
2811
"D"
1/4 TILE WIDTH
LINE BUFFER
2813
ODD
2815
"B"
3LL
3HL
3LH
3HH
2LL
AB
CD
Line
Buffer
2HL
2LH
2HH
1LL
AB
CD
Line
Buffer
1HL
1LH
1HH
PIXELS
AB
CD
LINE
BUFFER
X: ABCD ABCD ABCD...
YES: ABABAB....CDCDCD....

FIG. 28

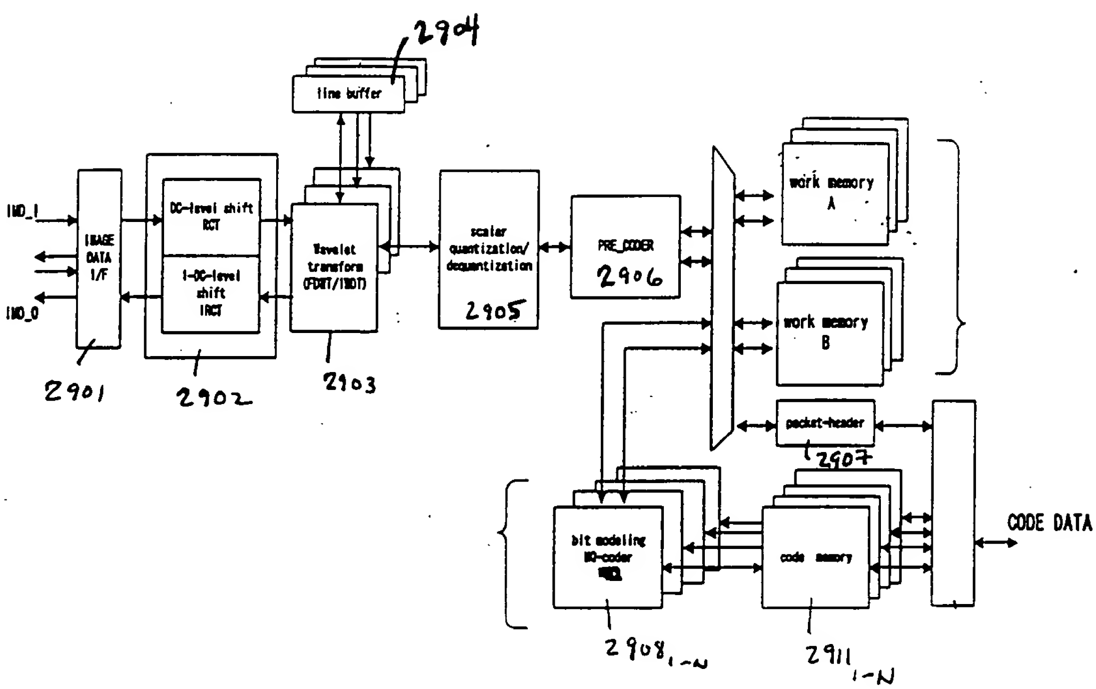

2904
line buffer
IMD_I
IMD_O
IMAGE DATA I/F
DC-level shift RCT
I-DC-level shift IRCT
Wavelet transform (FDWT/IDWT)
scalar quantization/ dequantization
2905
PRE_CODER
2906
work memory A
work memory B
packet-header
2907
bit modeling MQ-coder
code memory
CODE DATA
2901
2902
2903
2908 1-N
2911 1-N

Figure 29

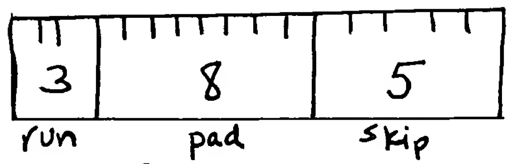


Figure 30

8x 8 region

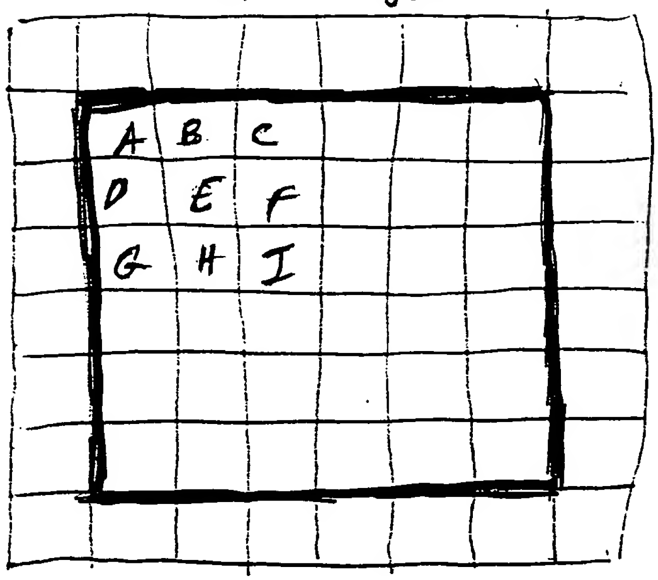


Figure 31

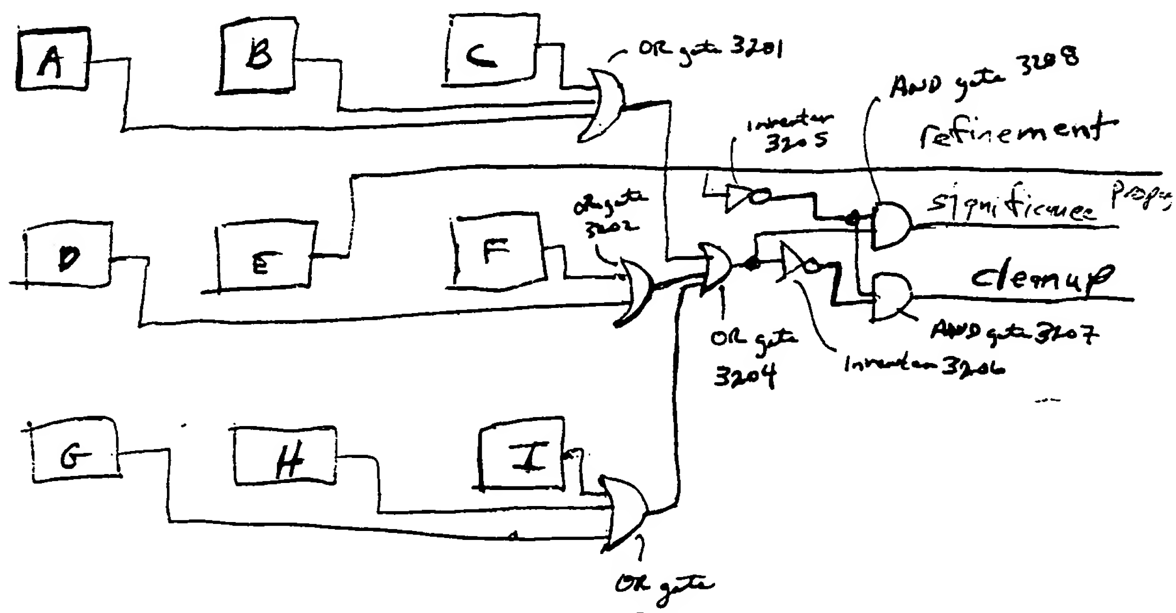


Figure 32